IN THE CLAIMS

Claims 1-28 are pending. Claims 1, 8, and 17 have been amended. A complete list of claims is presented below:

Current Listing of Claims

1. (Currently amended) A method comprising:

causing a first type of reset in a plurality of memory devices in a system in response to a second type of reset being initiated~~, different than the first type of reset,~~ in the system if the plurality of memory devices are not initialized, where the second type of reset is different than the first type of reset; and

enabling a deterministic shutdown mode in a memory controller coupled to the plurality of memory devices after the plurality of memory devices have been initialized.

2. (Original) The method of claim 1, further comprising:

putting the plurality of memory devices into a known state in response to the second type of reset being initiated in the system if the deterministic shutdown mode is enabled.

3. (Original) The method of claim 2, further comprising resetting in a plurality of stages a plurality of logic blocks in the memory controller while putting the plurality of memory devices into the known state.

4. (Original) The method of claim 3, further comprising resetting the memory controller after the plurality of memory devices have been put into the known state.

5. (Original) The method of claim 2, wherein the known state is a self-refresh state.

6. (Original) The method of claim 1, wherein the plurality of memory devices comprises one or more double data rate synchronous dynamic random access memory devices (DDR SDRAM).

7. (Original) The method of claim 1, wherein the first type of reset is a cold reset and the second type of reset is a warm reset.

8. (Currently Amended) An apparatus in a system comprising:

a switch to enable a deterministic shutdown mode when a plurality of memory devices in the system have been initialized;

a detector to detect a reset signal; and

a gate to gate the reset signal if the deterministic shutdown mode is enabled and to pass the reset signal to a logic unit if the deterministic shutdown mode is not enabled, wherein the plurality of memory devices go through a first type of reset in response to a second type of reset~~, different than the first type of reset,~~ being initiated in the system if the deterministic shutdown mode is not enabled, and the reset signal indicates that the second type of reset is being initiated in the system, where the second type of reset is different than the first type of reset.

9. (Original) The apparatus of claim 8, further comprising:

a sequencer, coupled to the detector, to cause the logic unit to put the plurality of memory devices into a known state in response to the second type of reset being initiated if the deterministic shutdown mode is enabled.

10. (Original) The apparatus of claim 9, wherein the sequencer causes the gate to pass the reset signal after the plurality of memory devices have been put into the known state.

11. (Original) The apparatus of claim 9, wherein the logic unit comprises a memory cycle tracker and command generator.

12. (Original) The apparatus of claim 11, wherein the sequencer receives one or more signals from the memory cycle tracker and command generator to determine whether the plurality of memory devices have been put into the known state.

13. (Original) The apparatus of claim 9, wherein the known state is a self-refresh state.

14. (Original) The apparatus of claim 9, further comprising a plurality of logic blocks, which are not used to put the plurality of memory devices into the known state and are reset in response to the second type of reset being initiated while the plurality of memory devices are being put into the known state.

15. (Original) The apparatus of claim 8, wherein the plurality of memory devices includes one or more double data rate synchronous dynamic random access memory devices (DDR SDRAM).

16. (Original) The apparatus of claim 8, wherein the first type of reset is a cold reset and second type of reset is a warm reset.

17. (Currently Amended) A computer system comprising:

a plurality of synchronous dynamic random access memory devices (SDRAM); and

a memory controller, coupled to the plurality of SDRAMs, comprising a switch to enable a deterministic shutdown mode when the plurality of SDRAMs have been initialized;

a detector to detect a reset signal; and

a gate to gate the reset signal if the deterministic shutdown mode is enabled and to pass the reset signal to a logic unit if the deterministic shutdown mode is not enabled, wherein the plurality of SDRAMs go through a first type of reset in response to a second type of reset~~, different than the first type of reset,~~ being initiated if the deterministic shutdown mode is not enabled, and the reset signal indicates that the second type of reset is being initiated, where the second type of reset is different than the first type of reset.

18. (Original) The computer system of claim 17, wherein the memory controller further comprises:

a sequencer, coupled to the detector, to cause the logic unit to put the plurality of SDRAMs into a known state in response to the second type of reset being initiated if the deterministic shutdown mode is enabled.

19. (Original) The computer system of claim 18, wherein the sequencer causes the gate to pass the reset signal after the plurality of SDRAMs have been put into the known state.

20. (Original) The computer system of claim 18, wherein the logic unit comprises a memory cycle tracker and command generator.

21. (Original) The computer system of claim 20, wherein the sequencer receives one or more signals from the memory cycle tracker and command generator to determine whether the plurality of SDRAMs have been put into the known state.

22. (Original) The computer system of claim 18, wherein the known state is a self-refresh state.

23. (Original) The computer system of claim 18, wherein the memory controller further comprises a plurality of logic blocks, which are not used to put the plurality of SDRAMs into the known state and are reset in response to the second type of reset being initiated while the plurality of SDRAMs are being put into the known state.

24. (Original) The computer system of claim 17, wherein the plurality of SDRAMs comprises one or more double data rate (DDR) SDRAMs.

25. (Original) The computer system of claim 17, wherein the first type of reset is a cold reset and the second type of reset is a warm reset.

26. (Original) The computer system of claim 17, further comprising a processor coupled to the memory controller.

27. (Original) The computer system of claim 26, wherein the processor initiates the second type of reset in response to a user request or a software application.

28. (Original) The computer system of claim 17, further comprising an input/output controller, coupled to the memory controller, to store a bit to indicate whether the plurality of SDRAMs are initialized.